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1 Introduction

This document describes failure cases where the ZSC31050 I^2C communication stops and the methods for restarting the communication again.

2 Failure Conditions

One of the conditions that could cause the ZSC31010 I^2C interface to block communication on the I^2C bus is if the master interrupts the communication without sending a stop condition. This can happen if there is an interruption in the microcontroller's supply.

The communication master microcontroller is supplied by a voltage in the range of 6V to 36V via a switching regulator. The ZSC31050 is also directly connected to this supply voltage via a JFET (e.g., BS169). If the supply voltage decreases to less than the 9V lower limit of the regulator, the microcontroller is switched off; however the ZSC31050, including the analog output, remains operational if the supply voltage remains within ZSC31050 specifications. If the supply voltage exceeds the 9V threshold again, the microcontroller will start communicating with the ZSC31050 again. In this case, the failure described above can occur; i.e., the ZSC31050 does not respond to I^2C requests. Typically this happens only after the supply voltage has crossed the 9V threshold multiple times.

A comparable condition can occur during EMC tests with the same consequence of interrupting I^2C communication.

2.1. Solution

Resetting the ZSC31050 is the recommended method for restarting I^2C communication. This is done by switching the supply voltage (and therefore the I^2C communication lines) off and then on. This procedure has no application restrictions.

A disadvantage of this procedure is that a highly complex circuitry solution is needed for powering off the supply voltage via a low-voltage controller as described in section 2.2. This work-a-round uses the VDD supply voltage instead of the analog supply voltage VDDA. This is especially needed in the non-ratiometric mode. This is a more cost-effective solution for resetting the ZSC31050.

Important: This application work-a-round is to be implemented by users at their own risk. IDT shall not be liable for any damages arising out of defects resulting from this work-a-round.

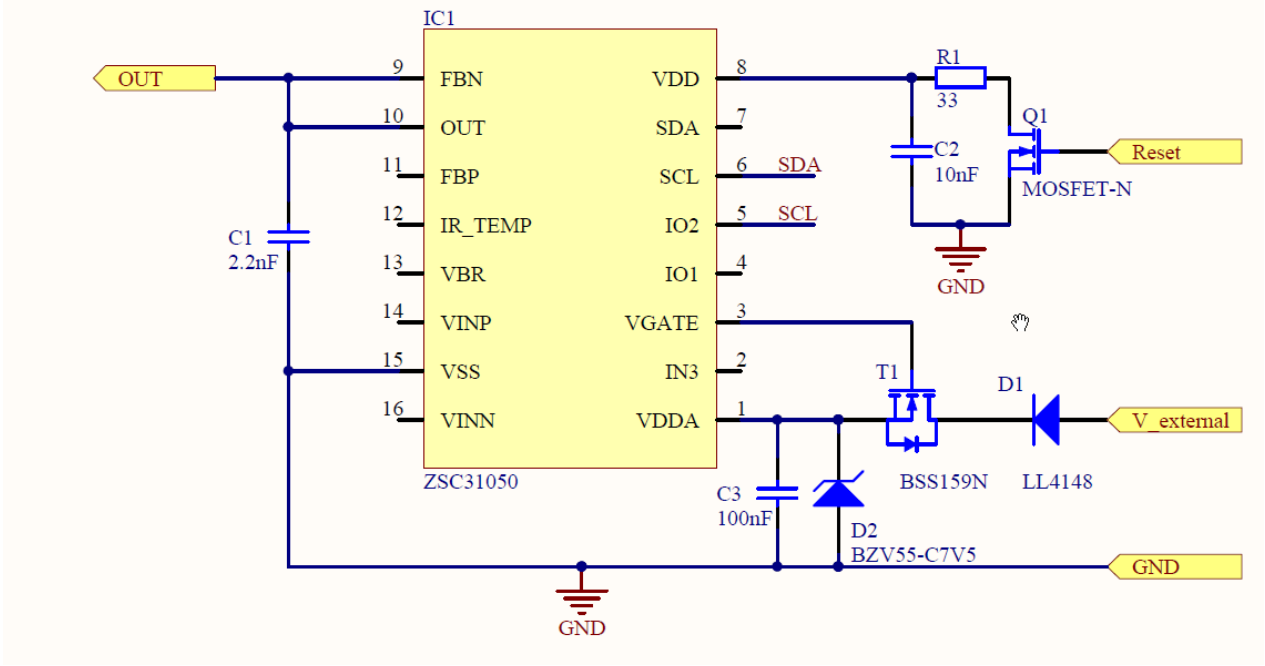
2.2. Solution Description and Technical Conditions

The reset is achieved by triggering a low-ohmic short from VDD to VSS via the circuit shown in Figure 2.1. The following conditions must be maintained during the procedure:

- The ambient temperature must be 25°C ± 15°C.
- The short resistor is R1=33Ω ± 10%.
- In absolute voltage output mode, the D2 Zener diode (V_Z = 6.8V) is required between the VDDA and VSS pins.
- The maximum activation/reset signal time must be < 0.25ms.
- The duty-cycle of the reset signal must be < $1/10^5$.
- Important: Using the work-a-round in continuous operation is not allowed. This means that the reset should not be used as a systematically activated function for this application.

Important: Additional application circuitry as described in the *ZSC31050 Datasheet* might be necessary.

Figure 2.1 Schematic for the Work-Around Circuit



The registers shown in Table 2.1 can be used to set and fine-tune the regulation of the ZSC31050 supply voltage.

Table 2.1 Register Configuration

Settings	Register	Register Name	Bits	Comment
Supply Voltage VDDA	18_{HEX}	CFGAPP	[1:2]	Coarse regulation
Supply Voltage VDDA	$1C_{HEX}$	ADJREF	[10:12]	Fine regulation

3 Related Documents

Visit the product page www.idt.com/zsc31050 on the IDT web site www.idt.com or contact your nearest sales office for the latest version of these documents.

Document
ZSC31050 Data Sheet
ZSC31050 Functional Description
SSC Evaluation Kit Description

4 Document Revision History

Revision	Date	Description
1.00	April 28, 2008	First release.
2.00	September 12, 2013	Changed to ZMDI template.
160601	June 1, 2016	Changed to IDT branding. Minor edits.

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