



Application Note

# Astra™ Machina Foundation Series SPI

Abstract: This application note provides detailed connection and guidelines of the Serial Peripheral Interface (SPI) with the SL1620, SL1640, SL1680, and SL2610 RDK.

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# 1. Overview

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The Serial Peripheral Interface (SPI) is a high-speed, full-duplex communication protocol widely used for interfacing microcontrollers, SoCs, and peripheral devices such as sensors, EEPROMs, ADCs, DACs, and display controllers. Astra RDK provides a built-in SPI controller that supports various modes, clock speeds, and multiple target devices (maximum four devices).

This application note focuses on the hardware design considerations for implementing SPI in Astra RDK-based designs, including SPI Boot mode.

The SL16x0 processor includes 2 SPI controllers. For SL1680 and SL1640, one of SPI operates on SM domain. Each SPI interface supports up to four target devices.

The SL2610 processor includes 5 SPI controllers. One of SPI operates on SM domain. The other four SPI interfaces each support up to four target devices.

The primary features of **SoC SPI** controller are:

- 4 CS pins
- SPI host and target mode (SL2610 SoC SPI only supports host mode)
- DMA mode
- Maximum SPI clock 50 MHz
- SPI mode 0, 1, 2, 3
- 1.8V I/O Voltage
- SPI Boot mode supported (SL16x0 with CS0 only)

The primary features of **SM SPI** controller are:

- 4 CS pins
- SPI host and target mode
- Maximum SPI clock 12.5 MHz (SL2610 SM SPI clock up to 25 MHz)
- SPI mode 0, 1, 2, 3
- 1.8V I/O Voltage

## 2. Hardware Connection of SPI1 (xSPI)

The SPI1 interface on the SL16xO RDK is connected to an on-board SPI flash (W25Q128JWSIQ) for SPI boot. The remaining three chip select (CS) pins are pin-muxed to other functions. Additionally, a 2×6 header is provided on the I/O board to facilitate connections with an external SPI key for debugging purposes.

For SL2610, it uses xSPI interface for boot. The hardware connection is like SL16xO RDK.

Figure 1 illustrates the location of the 2×6 header on the I/O board.

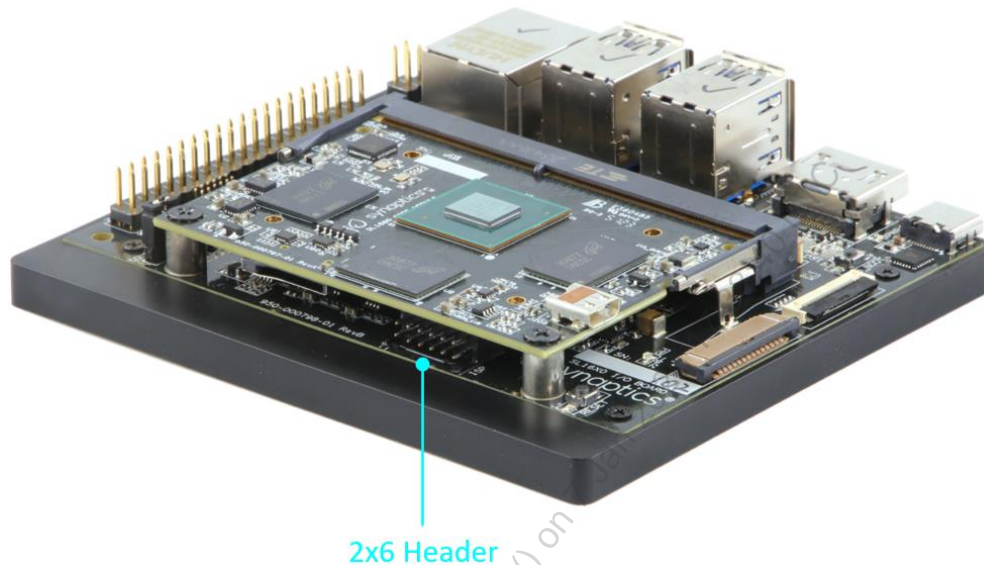


Figure 1. Overview of Astra Machina Foundation Series

### 2.1. Hardware Connection

Figure 2 illustrates the hardware connections of SPI1 on the SL16xO RDK and xSPI on the SL2610 RDK platform. The design enables seamless boot mode switching between on-board SPI Flash, external SPI key, and eMMC, ensuring flexible boot options.

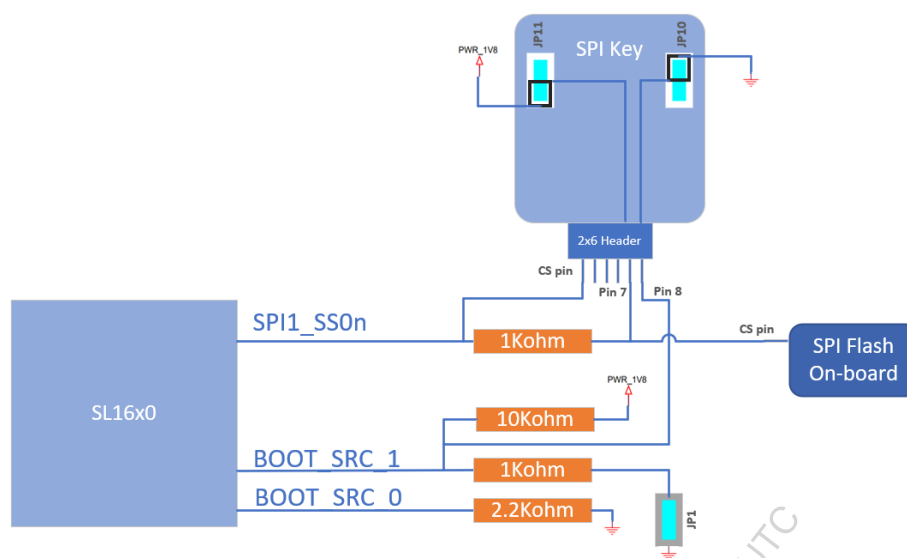


Figure 2. SPI1 connection of SL16x0 RDK

## 2.2. Boot mode of SL16x0 RDK

- **On-board SPI Boot**—SPI1 is connected to the on-board SPI Flash and is used as the primary boot source.
  - Leave 2x6 Header open
  - Short JP1
  - $BOOT\_SRC[1:0] = 2'b00$
- **External SPI Key Boot**—SPI1 is connected to both the on-board SPI Flash and the external SPI key. However, the chip select (CS) pin of the on-board SPI Flash is directly tied to 1.8V, effectively bypassing it and preventing it from being selected during communication.
  - JP10 to 2-3, JP11 to 2-3 on SPI board
  - JP1 no effect
  - $BOOT\_SRC[1:0] = 2'b00$
- **EMMC Boot:**
  - Leave 2x6 Header open
  - Leave JP1 open
  - $BOOT\_SRC[1:0] = 2'b10$

## 2.3. Boot mode of SL26x0 RDK

- **On-board SPI Boot**—xSPI is connected to the on-board SPI Flash and is used as the primary boot source.
  - Leave 2x6 Header open
  - Short JP1
  - $BOOT\_SRC[1:0] = 2'b01$
- **External SPI Key Boot**—xSPI is connected to both the on-board SPI Flash and the external SPI key. However, the chip select (CS) pin of the on-board SPI Flash is directly tied to 1.8V, effectively bypassing it and preventing it from being selected during communication.

- JP10 to 2-3, JP11 to 1-2 on SPI board
- Short JP1
- BOOT\_SRC[1:0] = 2'b01
- **EMMC Boot:**
  - Leave 2x6 Header open
  - Leave JP1 open
  - BOOT\_SRC[1:0] = 2'b10

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### 3. Hardware Connection of SPI2 on SL16x0 RDK

SPI2 is routed to the 40-pin header on the I/O board, enabling SPI peripheral expansion. To enhance compatibility with external SPI devices, the I/O voltage of SPI2 on the 40-pin header is converted to 3.3V using an on-board level shifter.

Figure 3 illustrates the location of SPI2 signals on the 40-pin header. Note that SPI2\_SS2n is allocated for another function on the board, leaving only three available chip select (CS) lines for SPI peripherals.


SL1680, SL1640/SL1620			
3.3V	1	2	5.0V
TW0 SDA	3	4	5.0V
TW0 SCL	5	6	GND
PWM[1]	7	8	UART0 Tx
GND	9	10	UART0 Rx
I2S2 BCLK/TW1 SCL	11	12	GPIO10/CM GPIO-EXP 0 2
I2S2 LRCK/TW1 SDA	13	14	GND
I2S2 DI[0]/I2S1 DI	15	16	ADCI[0]/PWM[2]
3.3V	17	18	ADCI[1]/GPIO2
SPI2 SDO	19	20	GND
SPI2 SDI	21	22	GPIO37/GPIO55
SPI2 CLK	23	24	SPI2 SS0n
GND	25	26	SPI2 SS1n
PDMB CLKIO/PDM CLKIO	27	28	PDMA DI[1]/PDM DI[1]
PDMA DI[0]/GPIO22	29	30	GND
GPIO39/GPIO48	31	32	GPIO38/GPIO47
GPIO36/CM GPIO-EXP 0 7	33	34	GND
I2S1 LRCK	35	36	SPI2 SS3n
I2S1 MCLK	37	38	I2S1 BCLK
GND	39	40	I2S1 DO[0]/I2S1 DO

Figure 3. SPI2 pin assignment on 40 pin Header

## 4. Hardware Connection of SM\_SPI1 on SL2610 RDK

In SL2610 RDK, SM\_SPI1 is routed to the 40-pin header on the I/O board, enabling SPI peripheral expansion. To enhance compatibility with external SPI devices, the I/O voltage of SM\_SPI1 on the 40-pin header is converted to 3.3V using an on-board level shifter.

Figure 4 illustrates the location of SM\_SPI1 signals on the 40-pin header. Note that SPI1\_SSn, SPI1\_SS1n and SPI1\_SS2n are allocated for other functions on the board, leaving only one available chip select (SPI1\_SS3n) lines for SPI peripherals.



SL2610					
3.3V	1	●	●	2	5.0V
TW2_SDA	3	●	●	4	5.0V
TW2_SCL	5	●	●	6	GND
SM_PWM2	7	●	●	8	SM_URTO_TX
GND	9	●	●	10	SM_URTO_RX
SM_GPIO27	11	●	●	12	SM_GPIO34
SM_GPIO26	13	●	●	14	GND
I2S2_DI	15	●	●	16	ADCI[0]
3.3V	17	●	●	18	ADCI[1]
SM_SPI1_SDO	19	●	●	20	GND
SM_SPI1_SDI	21	●	●	22	GPIO29
SM_SPI1_SCLK	23	●	●	24	SM_GPIO25
GND	25	●	●	26	SM_SPI1_SS3n
SM_PDM_CLKIO	27	●	●	28	SM_PDM_DIO
URT4_RXD	29	●	●	30	GND
URT4_TXD	31	●	●	32	SM_GPIO29
GPIO30	33	●	●	34	GND
I2S2_LRCK	35	●	●	36	SM_GPIO28
I2S2_MCLK	37	●	●	38	I2S2_BCLK
GND	39	●	●	40	I2S2_DO

Figure 4. SM\_SPI1 pin assignment on 40 pin Header

## 5. Registers of SPI controller

Table 1 provides the details of the SPI Controller registers.

Table 1. SPI Controller registers

Offset	Name	Description
0x00	CTRLR0	Control Register 0 This register controls the serial data transfer.
0x04	CTRLR1	Control Register 1 This register exists only when the DW_apb_ssi is configured as a host device. Control Register 1 controls the end of serial transfers when in receive-only mode.
0x08	SSIENR	SSI Enable Register This register enables and disables the DW_apb_ssi.
0x0C	MWCR	Microwire Control Register This register controls the direction of the data word for the half-duplex Microwire serial protocol.
0x10	SER	Target Enable Register This register is valid only when the DW_apb_ssi is configured as a host device. The register enables the individual target select output lines from the DW_apb_ssi host.
0x14	BAUDR	Baud Rate Select This register is valid only when the DW_apb_ssi is configured as a host device. The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the ssi_clk divider value.

## 5.1. Base address of each SPI controller

Table 2 lists the base address of SPI on each SL16x0 and SL2610 processor.

Table 2. Base Address of SPI registers

SoC	TWSI Controller	Base Address
SL1680	SPI1	0xF7E81C00
	SPI2	0xF7FCA000
SL1640	<b>SPI1</b>	0xF7E81C00
	SPI2	0xF7FCA000
SL1620	<b>SPI1</b>	0xF7E82C00
	SPI2	0xF7E83000
SL2610	SM SPI1	0x48034000
	SM SPI1_S	0x4803D000
	SPI2	0xF7F04000
	SPI3	0xF7F0B000
	SPI4	0xF7F0C000
	SPI5	0xF7F0D000

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## 6. References

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- *Astra Machina Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *SL1620 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001428-01)
- *SL1640 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001415-01)
- *SL1680 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001413-01)
- *SL2610 Embedded IoT Processor Electrical Specification Datasheet* (PN: 505-001501-01)
- *Astra Machina SL1620 Developer Kit User Guide* (PN: 511-001407-01)
- *Astra Machina SL1640 Developer Kit User Guide* (PN: 511-001405-01)
- *Astra Machina SL1680 Developer Kit User Guide* (PN: 511-001403-01)
- *Astra Machina SL2610 Developer Kit User Guide* (PN: 511-001453-01)

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## 7. Revision History

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Revision	Description
A	Initial release.
B	Added SL2610-related items.

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